What is claimed is:

1. A method of fabricating an input capacitance adjustment part in a semiconductor device, the method comprising the steps of:

providing a first conductivity type substrate in which first to third device isolation layers are formed;

forming a second conductivity type well having a first conductivity type impurity region inside between the first and second device isolation layers;

forming an active area to form a transistor between the second and third device isolation layers;

forming an oxide layer and a polysilicon layer on the entire structure successively;

forming a first area by patterning the oxide and polysilicon layers to remain on the first device isolation layer and thereby forming a gate on the active area;

forming source/drain regions in the first conductivity type substrate;

forming a first insulating interlayer on the entire structure;

forming contact holes by selectively removing predetermined portions of the first insulating interlayer formed on the drain region and the gate;

forming a first metal line on the entire structure including the contact holes;

forming a second area connected to the polysilicon layer of the first area and a predetermined portion of the impurity region, and a third area connected electrically with the impurity region and drain region and connected to an input buffer by patterning the first metal line;

forming a second insulating interlayer on the entire structure and then forming a second contact hole exposing a portion of the first area; and

forming a second metal line on the entire structure including the second contact hole and then forming an input pad by patterning the second metal line.

2. The method of claim 1, further comprising:

forming an internal-contact option layer in the first metal line of the second area so as to connect the polysilicon layer in the first area to the impurity region.

3. The method of claim 1, wherein a plurality of capacitors are formed by using the first conductivity type substrate, the first device isolation layer, and the polysilicon layer.

4. The method of claim 1, wherein the first conductivity type is a P-type conductivity, and the second conductivity type is an N-type conductivity.

5. A method of fabricating a semiconductor device, comprising the steps of:

forming first, second and third device isolation layers in a substrate;

forming a gate electrode having a polysilicon layer on the first device isolation layer;

forming source and drain regions between the second and third device isolation layers;

forming a first insulating layer over the gate electrode and over the source and drain regions;

forming an input pad layer on the insulating layer; and

forming a metal line layer underneath the polysilicon layer to either the input pad or a ground source.

6. The method of claim 5, wherein the polysilicon layer, the first device isolation layer and the substrate constitute a capacitor which is disposed underneath the input pad layer.

7. The method of claim 5, wherein the metal line layer is electrically connected to the input pad layer.

8. The method of claim 5, further comprising:

forming another insulating layer between the input pad layer and the first insulating layer.